



Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Original) A phase locked loop, comprising:
a feedback loop, the feedback loop including,
an integer divider operable to divide a feedback
loop signal in accordance with an integer divisor and produce a divided signal
having one
or more digital pulses;
a frequency multiplier operable to multiply the divided signal by a
multiplication
factor, including inserting one or more additional digital pulses into the divided
signal to
generate a multiplied signal; and
a re-sampling circuit operable to re-sample one or more of the additional
digital
pulses inserted into the divided signal if the multiplication factor does not divide
evenly
into the integer divisor.
2. (Original) The phase locked loop of claim 1, wherein the re sampling circuit is
operable to re-sample one or more of the additional digital pulses inserted into the divided signal
using one or more phase signals, each of the phase signals being delayed with respect to each
other.

3. (Original) The phase locked loop of claim 2, further comprising a multiphase voltage controlled oscillator operable to generate the one or more phase signals.

4. (Original) The phase locked loop of claim 2, wherein the re sampling circuit comprises a flip-flop that is clocked using one or more of the phase signals to re-sample one or more of the additional digital pulses.

5. (Original) The phase locked loop of claim 4, wherein the re sampling circuit further comprises a multiplexer that is operable to select a given phase signal to clock the flip flop.

6. (Original) The phase locked loop of claim 4, wherein the re sampling circuit further comprises a multiplexer that is operable to be controlled by a least significant bit of a binary value of the integer divisor for re-sampling one or more of the additional digital pulses.

7. (Original) The phase locked loop of claim 6, wherein the re sampling circuit further comprises an OR gate operable to insert one or more of the additional digital pulses into the divided signal.

8. (Original) The phase locked loop of claim 3, further comprising a phase-frequency detector operable to compare a reference signal to the multiplied signal, and generate an error signal corresponding to a frequency difference between the reference signal and the multiplied signal.

9. (Original) The phase locked loop of claim 8, further comprising a charge pump operable to convert the error signal into a charge pump output signal.

10. (Original) The phase locked loop of claim 9, further comprising a loop filter operable to smooth the charge pump output signal and generate a voltage controlled oscillator

control signal to control a frequency of an output signal of the multiphase voltage controlled oscillator.

11. (Original) The phase locked loop of claim 10, further comprising a programmable divider operable to divide the frequency of the output signal of the multiphase voltage controlled oscillator.

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20. (Original) A method comprising:
dividing a feedback loop signal in accordance with an integer divisor and
generating a divided signal having one or more digital pulses;
multiplying the divided signal by a multiplication factor, including inserting one
or more additional digital pulses into the divided output signal to generate a multiplied signal;
and
re-sampling one or more of the additional digital pulses inserted into the divided
signal if the multiplication factor does not divide evenly into the integer divisor.

21. (Original) The method of claim 20, wherein re-sampling one or more of the additional digital pulses includes re-sampling one or more of the additional digital pulses inserted into the divided signal using one or more phase signals, each of the phase signals being delayed with respect to each other.

22. (Original) The method of claim 21, wherein one or more of the phase signals are generated by a multiphase voltage controlled oscillator.

23. (Original) The method of claim 21, wherein re-sampling one or more of the additional digital pulses includes clocking a flip-flop using one or more of the phase signals.

24. (Original) The method of claim 23, wherein re-sampling one or more of the additional digital pulses further includes selecting a given phase signal to clock the flip-flop using a multiplexer.

25. (Original) The method of claim 23, further comprising using a least significant bit of a binary value of the integer divisor to control a multiplexer for re-sampling one or more of the additional digital pulses.

26. (Original) The method of claim 25, further comprising inserting one or more of the additional digital pulses into the divided signal using an OR gate.

27. (Original) The method of claim 22, further comprising comparing a reference signal to the multiplied signal, and generating an error signal corresponding to a frequency difference between the reference signal and the multiplied signal.

28. (Original) The method of claim 27, further comprising converting the error signal into a charge pump output signal.

29. (Original) The method of claim 28, further comprising smoothing the charge pump output signal and generating a voltage controlled oscillator control signal to control a frequency of an output signal of the multiphase voltage controlled oscillator.

30. (Original) The method of claim 29, further comprising dividing the frequency of the output signal of the multiphase voltage controlled oscillator.

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39. (Original) A disk drive system, comprising:

a read/write head configured to sense changes in magnetic flux on a surface of a disk according to a control signal supplied by a phase locked loop (PLL) and generate a corresponding analog signal, the PLL including,

an integer divider operable to divide a feedback loop signal in accordance with an

integer divisor and produce a divided signal having one or more digital pulses;

a frequency multiplier operable to multiply the divided signal by a multiplication

factor, including inserting one or more additional digital pulses into the divided signal to

generate a multiplied signal; and

a re-sampling circuit operable to re-sample one or more of the additional digital

pulses inserted into the divided signal if the multiplication factor does not divide evenly

into the integer divisor;

the disk drive system further comprising a preamplifier configured to amplify the analog signal; and

a read channel configured to receive the amplified analog signal and generate a digital read signal based on the amplified analog signal.

40. (Original) The disk drive system of claim 39, wherein the re sampling circuit is operable to re-sample one or more of the additional digital pulses inserted into the divided signal using one or more phase signals, each of the phase signals being delayed with respect to each other.

41. (Original) The disk drive system of claim 40, wherein the PLL further includes a multiphase voltage controlled oscillator operable to generate the one or more phase signals.

42. (Original) The disk drive system of claim 40, wherein the re sampling circuit comprises a flip-flop that is clocked using one or more of the phase signals to re-sample one or more of the additional digital pulses.

43. (Original) The disk drive system of claim 42, wherein the re sampling circuit further comprises a multiplexer that is operable to select a given phase signal to clock the flip flop.

44. (Original) The disk drive system of claim 42, wherein the re sampling circuit further comprises a multiplexer that is operable to be controlled by a least significant bit of a binary value of the integer divisor for re-sampling one or more of the additional digital pulses.

45. (Original) The disk drive system of claim 44, wherein the re sampling circuit further comprises an OR gate operable to insert one or more of the additional digital pulses into the divided signal.

46. (Original) The disk drive system of claim 41, wherein the PLL further includes a phase-frequency detector operable to compare a reference signal to the multiplied signal, and generate an error signal corresponding to a frequency difference between the reference signal and the multiplied signal.

47. (Original) The disk drive system of claim 46, wherein the PLL further includes a charge pump operable to convert the error signal into a charge pump output signal.

48. (Original) The disk drive system of claim 47, wherein the PLL further includes a loop filter operable to smooth the charge pump output signal and generate a voltage controlled oscillator control signal to control a frequency of an output signal of the multiphase voltage controlled oscillator.

49. (Original) The disk drive system of claim 48, wherein the PLL further includes a programmable divider operable to divide the frequency of the output signal of the multiphase voltage controlled oscillator.

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58. (Original) A phase locked loop, comprising:

feedback means including,

means for dividing a feedback loop signal in accordance with an integer
divisor

and producing a divided signal having one or more digital pulses;

means for multiplying the divided signal by a multiplication factor,
including

inserting one or more additional digital pulses into the divided signal and
generating a

multiplied signal; and

means for re-sampling one or more of the additional digital pulses inserted into the divided signal if the multiplication factor does not divide evenly into the integer divisor.

59. (Original) The phase locked loop of claim 58, wherein the means for re-sampling is operable to re-sample one or more of the additional digital pulses inserted into the divided signal using one or more phase signals, each of the phase signals being delayed with respect to each other.

60. (Original) The phase locked loop of claim 59, further comprising generating means for generating the one or more phase signals.

61. (Original) The phase locked loop of claim 59, wherein the means for re-sampling is clocked using one or more of the phase signals for re-sampling one or more of the additional digital pulses.

62. (Original) The phase locked loop of claim 61, wherein the means for re-sampling further comprises selector means for selecting a given phase signal to clock the means for re-sampling.

63. (Original) The phase locked loop of claim 61, wherein the means for re-sampling further comprises selector means that is operable to be controlled by a least significant bit of a binary value of the integer divisor for re-sampling one or more of the additional digital pulses.

64. (Original) The phase locked loop of claim 63, wherein the means for re-sampling further comprises means for inserting one or more of the additional digital pulses into the divided signal.

65. (Original) The phase locked loop of claim 60, further comprising means for comparing a reference signal to the multiplied signal, and generating an error signal corresponding to a frequency difference between the reference signal and the multiplied signal.

66. (Original) The phase locked loop of claim 65, further comprising means for converting the error signal into a charge pump output signal.

67. (Original) The phase locked loop of claim 66, further comprising means for smoothing the charge pump output signal and generating a control signal to control a frequency of an output signal of the generating means.

68. (Original) The phase locked loop of claim 67, further comprising means for dividing the frequency of the output signal of the generating means.

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77. (Original) A disk drive system, comprising:
sensing means for sensing changes in magnetic flux on a surface of a disk according to a control signal supplied by a phase locking means and generating a corresponding analog signal, the phase locking means including,
dividing means for dividing a feedback loop signal in accordance with an integer divisor and producing a divided signal having one or more digital pulses;

multiplying means for multiplying the divided signal by a multiplication factor,
including inserting one or more additional digital pulses into the divided signal
and
generating a multiplied signal; and
re-sampling means for re-sampling one or more of the additional digital pulses
inserted into the divided signal if the multiplication factor does not divide evenly
into the
integer divisor;
the disk drive system further comprising means for amplifying the analog signal;
and
means for receiving the amplified analog signal and generating a digital read signal based on the amplified analog signal.

78. (Original) The disk drive system of claim 77, wherein the re sampling means is operable to re-sample one or more of the additional digital pulses inserted into the divided signal using one or more phase signals, each of the phase signals being delayed with respect to each other.

79. (Original) The disk drive system of claim 78, wherein the phase locking means further includes generating means for generating the one or more phase signals.

80. (Original) The disk drive system of claim 78, wherein the re sampling means is clocked using one or more of the phase signals for re-sampling one or more of the additional digital pulses.

81. (Original) The disk drive system of claim 80, wherein the re sampling means further comprises selector means for selecting a given phase signal to clock the means for re sampling.

82. (Original) The disk drive system of claim 80, wherein the re sampling means further comprises selector means that is operable to be controlled by a least significant bit of a binary value of the integer divisor for re-sampling one or more of the additional digital pulses.

83. (Original) The disk drive system of claim 82, wherein the re sampling means further comprises means for inserting one or more of the additional digital pulses into the divided signal.

84. (Original) The disk drive system of claim 79, wherein the phase locking means further includes means for comparing a reference signal to the multiplied signal, and generating an error signal corresponding to a frequency difference between the reference signal and the multiplied signal.

85. (Original) The disk drive system of claim 84, wherein the phase locking means further includes means for converting the error signal into a charge pump output signal.

86. (Original) The disk drive system of claim 85, wherein the phase locking means further includes means for smoothing the charge pump output signal and generating a control signal to control a frequency of an output signal of the generating means.

87. (Original) The disk drive system of claim 86, wherein the phase locking means further includes programmable means for dividing the frequency of the output signal of the generating means.

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- 89. Cancelled
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- 92. Cancelled

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